IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant	: Hisashi Ohtani	Art Unit :	2822
Serial No.	: 10/657,137	Examiner :	Ida M. Soward
Filed	: September 9, 2003	Confirmation No.:	1909
		Notice of Allowance Date:	August 8, 2005

Title : SEMICONDUCTOR INTEGRATED CIRCUIT AND FABRICATION METHOD THEREOF

MAIL STOP ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

RESPONSE TO NOTICE OF ALLOWANCE

In response to the Notice of Allowance mailed August 8, 2005, enclosed are a completed issue fee transmittal form PTOL-85b and a check for $1730 for the required issue fee and publication fee, including patent copies.

Please apply any additional charges or credits to our Deposit Account No. 06-1050.

Respectfully submitted,

Date: November 7, 2005

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